AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A data processing device formed as a semiconductor integrated circuit to be coupled to an external device for performing data transmission and reception, said data processing device comprising:

a central processing unit ~~operated at a first voltage~~; and

an interface unit for data transmission and reception to and from the external device,

wherein said interface unit includes:

an external clock output terminal for outputting a clock signal;

an output driver for driving said external clock output terminal to output said clock signal; ~~and~~

a load circuit capable of imparting, to the clock signal extracted from a position in a stage previous to said output driver in a clock signal path, a variable delay in accordance with a delay resulting from an external load coupled to said external clock output terminal in order to generate a delayed clock signal; ~~for latching data inputted~~

~~from the external device, wherein both the output driver and the load circuit operate at a second voltage higher than said first voltage.~~

an external data input terminal for inputting external data; and

a data latch circuit for latching said external data in accordance with said delayed clock signal.

2. (previously presented) A data processing device according to claim 1, wherein said load circuit is a time constant circuit comprising resistors and capacitors.

3. (currently amended) A data processing device according to claim 2,

wherein said load circuit comprises a plurality of time constant circuits to generate a plurality of clock signals with different amounts of delay, and selects any of the plurality of clock signals as the delayed clock signal for latching said external~~the~~ data ~~inputted from the external device~~.

4. (currently amended) A data processing device formed as a semiconductor integrated circuit to be coupled to an external memory device for performing data

transmission and reception, said data processing device comprising:

a central processing unit ~~operated at a first voltage~~;

a clock pulse generation circuit capable of generating different clock pulse signals; and

an interface unit for data transmission and reception to and from the external memory device,

wherein said interface unit includes:

an~~a first~~ external clock output terminal for outputting a clock signal derived from a clock pulse signal generated by the clock pulse generation circuit;

an output driver for driving said ~~first~~ external clock output terminal to output said clock signal; ~~and~~

a load circuit capable of imparting, to the clock signal extracted from a position in a stage previous to said output driver in a clock signal path, a variable delay in accordance with a delay resulting from an external load coupled to said ~~first~~ external clock output terminal;~~,~~ ~~wherein both the output driver and the load circuit operate at a second voltage higher than said first voltage;~~

a plurality of ~~second~~ external data input terminals for receiving data from the external memory device; and

a plurality of latch circuits ~~operated at said first voltage~~ for latching data received by said plurality of ~~second~~ external data input terminals,

wherein said latch circuits latch data based on the clock signal as delayed by said load circuit.

Claims 5-6 (cancelled)

7. (previously presented) A data processing device according to claim 4, wherein said load circuit includes a time constant circuit comprising resistors and capacitors.

8. (previously presented) A data processing device according to claim 4,

wherein said load circuit includes a plurality of time constant circuits, generates a plurality of clock signals with different amounts of delay, and selects any of the plurality of clock signals for latching data inputted from the external memory device.

9. (currently amended) A data processing device according to claim 8, wherein said load circuit includes:

a selector circuit ~~operated at said second voltage~~ which selects a signal passing through or not passing

through any of the plurality of time constant circuits as the clock signal for latching data inputted from the external memory device.

10. (currently amended) A data processing device according to claim 9, further comprising:

a register ~~operated at said first voltage~~ which stores a set value for determining a state of said selector circuit; and

a decoder ~~operated at said second voltage~~ which generates a control signal for said selector circuit in accordance with the set value of the register.

11. (currently amended) An electronic device comprising:

a data processing device as recited in claim 1; and

a nonvolatile memory device capable of coupling to the data processing device,

wherein said nonvolatile memory device performs data transmission and reception based on said clock signal outputted from said external clock output terminal of said data processing device.

12. (new) A data processing device according to claim 1, wherein said load circuit extracts the clock signal from a stage immediately preceding said output driver.

13. (new) A data processing device according to claim 4, wherein said load circuit extracts the clock signal from a stage immediately preceding said output driver.